REMARKS

The Office Action dated April 22, 2005, has been received and reviewed.

Claims 1-12 are currently pending and under consideration in the above-referenced application. Each of claims 1-12 stands rejected.

New claims 13 and 14 have been added.

Reconsideration of the above-referenced application is respectfully requested.

Rejections Under 35 U.S.C. § 103(a)

Claims 1-12 stand rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over that taught in U.S. Patent No. 6,594,542 to Williams (hereinafter "Williams"), in view of teachings from U.S. Patent No. 6,725,120 to Saldana (hereinafter "Saldana").

The standard for establishing and maintaining a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Williams teaches methods for determining the length of time that a polishing pad should be used at a particular pressure and with a particular slurry to remove a desired amount (*i.e.*, thickness) of material from a substrate, such as a semiconductor wafer. The method of Williams includes, among other things, consideration of prior use (*e.g.*, wear) of the polishing pad.

Saldana teaches a technique in which accurate CMP-related calculations, including pressure and forces to be applied as a polishing pad moves over a wafer and wafer carrier, may be made without high resolution components. FIGs. 1A-1D of Saldana illustrate a system 200

that includes a polishing pad 220 and a "setup" over which the polishing pad 220 is positioned. The "setup" includes a wafer carrier, which includes a ring 224 that laterally retains a wafer 204, as well as a conditioning puck 222. Col. 9, lines 7-11. Force actuators 239W, 239R, and 239C are associated with the backsides of the wafer carrier and the puck 222, respectively. Col. 9, lines 54-63. The wafer carrier is apparently configured to apply a constant amount of force across the backside of the wafer 204, while the force actuator 239W associated with the wafer carrier applies force to the wafer carrier. *Id.* The force actuators 239R and 239C associated with the ring 224 and puck 222 are likewise configured to apply force to the ring 224 and puck 222. *Id.*

It is respectfully submitted that a *prima facia* case of obviousness under 35 U.S.C. § 103(a) has not been established against claims 1-12. In particular, it is respectfully submitted that neither Williams nor Saldana teaches or suggests each and every element of any of claims 1-12.

With respect to the subject matter recited in independent claim 1, neither Willians nor Saldana teaches or suggests "applying [a] force gradient to a backside of at least one . . . semiconductor device structure . . ." Rather, Williams and Saldana teach nothing more than applying a constant force to the backsides of wafers.

The only force gradients that are generated in Saldana are force gradients on the polishing pad 220, which are caused by differences between the amounts of force applied to the ring 224, the conditioning puck 222, and the wafer 204 by way of the force actuators 239R, 239C, and 239W, respectively.

Further, while a force gradient may be applied directly against the wafer 204 itself, that force gradient is present on the active surface of the wafer. It is a two-step gradient that is generated only because the polishing pad contacts a portion of the active surface, while no force is applied to the part of the wafer not in contact with the polishing pad.

Each of claims 2-7 is allowable, among other reasons, for depending either directly or indirectly from claim 1, which are allowable.

Claim 5 is additionally allowable because Williams and Saldana both lack any teaching or suggestion of "determining amounts of force to apply to at least two areas of the backside of . . .

at least one . . . semiconductor device structure so as to facilitate the formation of a substantially planar active surface of the at least one . . . semiconductor device structure during polishing thereof." Instead, Williams notes that material may be removed more quickly from some locations of a semiconductor device structure than from other locations, but does not teach or suggest the application of differential force to account for differences in material removal rates. Saldana is likewise silent as to applying differential force in consideration of the heights of raised areas to be polished and the rate at which material is removed lower areas.

Claim 6 is additionally allowable because neither Williams nor Saldana includes any teaching or suggestion of applying at least two different amounts of pressure to a backside of a semiconductor device structure.

Independent claim 8 is drawn to a method for compensating for nonplanarities on an active surface of a semiconductor device structure. The method of independent claim 8 includes, among other things, "selectively applying increased amounts of pressure to at least two locations on a backside of at let one semiconductor device structure relative to pressure applied to other areas of the backside . . ."

Williams and Saldana both lack any teaching or suggestion of selectively applying different amounts of pressure to different locations on the backside of a semiconductor device structure. Rather, the teachings of Williams relate solely to processes for compensating for changes in the ability of a polishing pad to remove materials, while the teachings of Saldana are limited to applying two different amounts of pressure to the active surface of a wafer 204 with a polishing pad 220 (*i.e.,* no pressure at locations that are not contacted by the polishing pad 220 and some pressure at locations that are contacted by the polishing pad 220).

As neither Williams nor Saldana, taken either individually or collectively, teaches or suggests each and every element of independent claim 8, it is respectfully submitted that a *prima facie* case of obviousness has not been established against the subject matter recited in independent claim 8. Thus, under 35 U.S.C. § 103(a), the subject matter to which independent claim 8 is drawn is allowable over the teachings of Williams and Saldana.

Claims 9-12 are each allowable, among other reasons, for depending directly or indirectly from claim 8, which is allowable.

Claim 9 is also allowable since Williams and Saldana both include no teaching or suggestion of applying a pressure gradient to a backside of a semiconductor device structure.

Claim 10, which depends from claim 9, is further allowable because neither Williams nor Saldana teaches or suggests generating a pressure gradient based on the height of at least one raised area and the rate at which material is removed from a lower area of the semiconductor device structure.

For these reasons, withdrawal of the 35 U.S.C. § 103(a) rejections of claims 1-12 is respectfully solicited.

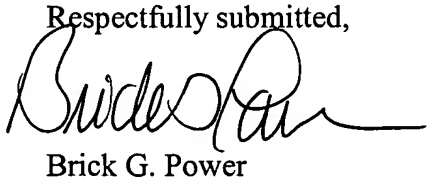
New Claims

New claims 13 and 14 have been added. New claims 13 and 14 respectively depend from claims 1 and 8, and recite that different amounts of force or pressure are simultaneously applied to a backside of a semiconductor device structure. Neither new claim 13 nor new claim 14 introduces new matter into the above-referenced application.

CONCLUSION

It is respectfully submitted that each of claims 1-14 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



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